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ORIGINAL

PATENT APPLICATION

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AF/2181

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Gregory E. BURNS et al.

Confirmation No.: 4281

Application No.: 09/629,601

Examiner: R. N. Phan

Filing Date: 07/31/2000

Group Art Unit: 2181

Title: CONFIGURABLE STORAGE ARRAY ADAPTED TO CONFIGURE A SEGMENTABLE BUS BASED ON AN ARRANGEMENT OF CONNECTORS (AS AMENDED)

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith in **triplicate** is the Appeal Brief in this application with respect to the Notice of Appeal filed on 01/16/2004.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $330.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$110.00
( )	two months	$420.00
( )	three months	$950.00
( )	four months	$1480.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of $330.00. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: 03/15/2004

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Respectfully submitted,

Gregory E. BURNS et al.

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ORIGINAL #12 3-24-04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Gregory E. BURNS et al.	§	Confirmation No.:	4281
Serial No.:	09/629,601	§	Group Art Unit:	2181
Filed:	07/31/2000	§	Examiner:	R. N. Phan
For:	Configurable Storage Array Adapted to Configure A Segmentable Bus Based On An Arrangement Of Connectors (As Amended)	§	Docket No.:	200301760-1

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: March 15, 2004

Sir:

Appellant hereby submits this Appeal Brief in connection with the above-identified application. A Notice of Appeal was filed on January 16, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is the Hewlett-Packard Company through its merger with Compaq Computer Corporation which owned Compaq Information Technologies Group, L.P. (CITG).

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

Originally filed claims:	1-25.
Claim cancellations:	None.
Added claim:	None.
Presently pending claims:	1-25.
Presently appealed claims:	1-25.

IV. STATUS OF THE AMENDMENTS

Applicants did not file any amendments after the final rejection.

V. SUMMARY

At least some electronic and computing systems include one or more storage devices to which computers, such as servers, can interact to store and retrieve data. Disclosure page 2. In some systems, storage devices are grouped into storage "arrays" to provide centralized storage and backup capabilities. Disclosure pages 3-4. Setting up and configuring such storage systems can be complicated. Configuration issues, such as electrical termination, complicate the design and versatility of many systems having storage arrays. Disclosure page 4. Further complications arise the inclusion of "hot plug" storage devices into a system.

In at least one embodiment described at least from page 9, line 16, through page 12, line 8 and in conjunction with Figures 2A, 2B and 3, Applicants' contribution comprises a system in which one or more storage devices 60 can be coupled to a backplane 110. A segmentable bus 140 couples to the various storage devices and to a plurality of input/output ("I/O") connectors 70-76. Control logic 170 is adapted to determine an arrangement of connectors (e.g., Figures 2A and 2B connectors 25, 35, 45) coupled to the I/O connectors and to configure the segmentable bus to define a plurality of storage device arrays based on the arrangement.

Claim 1 exemplifies at least one embodiment of the invention and is as follows:

1. A configurable storage array, comprising:
   a backplane;
   a plurality of storage devices coupled to the backplane;
   a segmentable bus coupled to the storage devices;
   a plurality of input/output connectors coupled to the segmentable bus; and
   a control board including control logic adapted to determine an arrangement of connectors coupled to the input/output connectors

and configure the segmentable bus to define a plurality of storage device arrays based on the arrangement.

VI. ISSUE(S)

1. Whether claim 1 is patentable under 35 U.S.C. § 102(e) over Mulvihill (U.S. Pat. No. 6,516,370).
2. Whether claims 2-25 are patentable under 35 U.S.C. § 103 over Mulvihill in view of Sicola (U.S. Pat. No. 5,938,776).

VII. GROUPING OF CLAIMS

Applicants contend that independent claims 1, 15, and 25 are patentable for separate reasons as argued below. For purposes of this Appeal only, the dependent claims stand or fall with their respective independent claims.

VIII. ARGUMENT

A. The Mulvihill Reference

Mulvihill is directed to a data storage system that has "redundancy arrangements to protect against a total system failure in the event of a failure in a component or subassembly of the storage system." Col. 1, lines 5-10. Mulvihill discloses a system interface 16 which couples a host computer 12 to a plurality of storage devices 80. The Examiner focused on language in columns 4-6 of Mulvihill. In that section of the patent, Mulvihill discloses the following with reference to Figure 1:

> In operation, when the host computer 12 wishes to store data, the host computer 12 issues a write request to one of the front-end directors 20_4 -20_{11} to perform a write command. One of the front-end directors 20.sub.4 -20.sub.11 replies to the request and asks the host computer 12 for the data. After the request has passed to the requesting one of the front-end directors 20_4 -20_{11}, the director determines the size of the data and reserves space in the cache memory 18 to store the request.... The host computer 12 then transfers the data to the front-end director. The front-end director then advises the host computer 12 that the transfer is complete. The front-end director looks up in a Table, not shown, stored in the cache memory 18 to determine which one of the rear-end directors 20_0 -20_3 and 20_{12} -20_{15} is to handle this request. The Table maps the host computer 12 addresses into an address in the bank 14 of disk drives. The front-end director then puts a notification in a "mail box" (not shown and stored in the cache memory 18) for the rear-end director which is to handle the request, the amount of the data and the disk

address for the data. Other rear-end directors poll the cache memory 18 when they are idle to check their "mail boxes". If the polled "mail box" indicates a transfer is to be made, the rear-end director processes the request, addresses the disk drive in the bank, reads the data from the cache memory and writes it into the addresses of a disk drive in the bank 14. When data is to be read from the disk drive to the host computer 12 the system operates in a reciprocal manner.

B. The Sicola Reference

Sicola is generally related to detecting small computer system interface ("SCSI") devices installed at illegal locations on a SCSI bus. In particular, the subject matter of Sicola relates to detecting in a mixed environment of eight-bit SCSI devices and 16-bit SCSI devices the eight-bit SCSI device installed at locations intended for 16-bit SCSI devices. See column 1, lines 7-12.

C. The Examiner Erred in Rejecting Claim 1 as Anticipated by Mulvihill

Claim 1 is directed to a configurable storage array having, among other features, a plurality of input/output connectors coupled to a segmentable bus. The storage array also comprises "control logic adapted to determine an arrangement of connectors coupled to the input/output connectors and configure the segmentable bus to define a plurality of storage device arrays based on the arrangement." The Examiner alleges that the "control logic" limitation is taught at column 4, lines 40-65 of Mulvihill. Final Office Action page 3. The Examiner also refers to language from columns 5 and 6 of Mulvihill. None of the referenced language from Mulvihill teaches or even suggests a "segmentable bus" as claimed much less "control logic adapted to determine an arrangement of connectors coupled to the input/output connectors and configure the segmentable bus to define a plurality of storage device arrays based on the arrangement." Mulvihill does not teach or suggest a segmentable bus that can be configured depending on the arrangement of connectors coupled to the I/O connectors.

The passages to which the Examiner referred simply do not teach or even suggest the limitations quoted above. Mulvihill does not teach that the system interface 16 is in any way configurable based on an arrangement of any connectors. The Examiner thus erred in rejecting claim 1 as anticipated over Mulvihill.

Despite the genuine efforts of the Examiner, Applicants have found the prosecution of this case somewhat difficult because the Examiner's application of Mulvihill to the claims is unclear and generally off base. For the "control logic" limitation, the Examiner referred to column 4, lines 40-65 of Mulvihill which states:

> Referring now to FIG. 1, a data storage system 10 is shown wherein a host computer 12 is coupled to a bank 14 of disk drives through a system interface 16. The system interface 16 includes a cache memory 18, having a high memory address section 18H and a low address memory section 18L. A plurality of directors 20_0 -20_{15} is provided for controlling data transfer between the host computer 12 and the bank 14 of disk drives as such data passes through the cache memory 18. A pair of high address busses TH, BH is electrically connected to the high address memory sections 18H. A pair of low address busses TL, BL electrically connected to the low address memory sections 18L. The cache memory 18 has a plurality of storage location addresses. Here, the storage locations having the higher addresses are in the high address memory sections 18H and the storage locations having the lower addresses are in the low address memory sections 18L. It should be noted that each one of the directors 20_0 –20_{15} is electrically connected to one of the pair of address busses TH, BL and one to the other of the pair of address busses TL, BH, as indicated. It is also noted that each one of the directors 20_0 –20_{15} is able to address all locations in the entire cache memory 18 (i.e., to both the high address memory section 18H and the low address memory section 18L) and is therefore able to store data in and retrieve data from any storage location in the entire cache memory 18.

Applicants remained, and still remain, stumped as to why the Examiner believes this passage teaches the claimed "control logic adapted to determine an arrangement of connectors coupled to the input/output connectors and configure the segmentable bus to define a plurality of storage device arrays based on the arrangement." In a Response filed September 11, 2003, Applicants requested clarification. In the Final Office Action, page 7, the Examiner repeated the same argument, but offered the following response to Applicants' contention that Mulvihill is devoid of a teaching of the claimed "control logic":

> Mulvihill et al. teach host computer 12 is coupled to the bank 14 of the disk drives through the system interface 16 having a high memory section 18H and low memory section 18L (see col. 4, lines 40-50); each of the director coupled to the segmentable bus 18 and

> each disk drive coupled to the I/O adapter which has the primary port and second port (see col. 5, lines 38-58); the system interface determine the location of the I/O ports and the define the plurality of input/output connectors base on the location (see col. 5, line 60 through col. 6, line 35).

The passage from columns 4 and 5 to which the Examiner refers simply does not teach the "control logic" limitation. Mulvihill does not at all teach configuring a segmentable bus to define a plurality of storage device arrays based on how a user couples connectors to the segmentable bus connectors. With all due respect to the Examiner, the Examiner's arguments regarding this feature of claim 1 appear to be largely irrelevant.

Further, the Examiner referred to "segmentable bus 18" in the quoted passage above. In Figure 1 of Mulvihill, the reference number 18 identifies a cache memory, not a bus. The Examiner's rejection should be reversed for at least this reason as well.

D. The Examiner Erred in Rejecting Claims 2-25 as Obvious Over Mulvihill in View of Sicola

In addition to not being anticipated by Mulvihill, for the reasons stated above, claim 1 also is not obvious over Mulvihill. The Examiner used Sicola in the obviousness rejections of claims 2-25. Sicola does not teach or even suggest "control logic adapted to determine an arrangement of connectors coupled to the input/output connectors and configure the segmentable bus to define a plurality of storage device arrays based on the arrangement" as required by claim 1. Sicola does not satisfy the deficiency of Mulvihill. For these reasons, claim 1 is allowable over Mulvihill and Sicola. Claims 2-14 depend on or from claim 1. At least because claim 1 is patentable over Mulvihill and Sicola, the Examiner erred in rejecting claims 2-14.

Independent claim 15 is directed to a method that comprises "determining an arrangement of connectors coupled to input/output connectors of the storage array" and "grouping subsets of the storage devices onto isolated bus segments in the storage array based on the arrangement of connectors." Neither Mulvihill nor Sicola teaches or suggests this combination of limitations as explained above.

For at least this reason, the Examiner erred in rejecting claim 15 and its dependent claims.

Clam 25 is directed to an apparatus comprising a "means for determining an arrangement of connectors coupled to input/output connectors of the storage array" and a "means for grouping subsets of the storage devices onto isolated bus segments based on the arrangement of connectors." As explained previously, neither Mulvihill nor Sicola teaches or suggests this combination of limitations. For at least this reason, the Examiner erred in rejecting claim 25.

IX. CONCLUSION

For the reasons stated above, Applicants respectfully submit that the Examiner erred in rejecting all pending claims. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Respectfully submitted,

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APPENDIX TO APPEAL BRIEF

CURRENT CLAIMS

1. (Original) A configurable storage array, comprising:

a backplane;

a plurality of storage devices coupled to the backplane;

a segmentable bus coupled to the storage devices;

a plurality of input/output connectors coupled to the segmentable bus; and

a control board including control logic adapted to determine an arrangement of connectors coupled to the input/output connectors and configure the segmentable bus to define a plurality of storage device arrays based on the arrangement.

2. (Original) The configurable storage array of claim 1, wherein the control logic is adapted to determine the arrangement of connectors and configure the segmentable bus upon power up of the configurable storage array.

3. (Original) The configurable storage array of claim 1, wherein the control board includes a reconfiguration switch, and the control logic is adapted to determine the arrangement of connectors and configure the segmentable bus upon activation of the reconfiguration switch.

4. (Original) The configurable storage array of claim 1, wherein the control board includes a plurality of expanders separating portions of the segmentable bus.

5. (Original) The configurable storage array of claim 4, wherein the control logic is adapted to selectively activate particular ones of the expanders based on the arrangement of connectors.

6. (Original) The configurable storage array of claim 4, wherein the control logic is adapted to disable one of the expanders on a portion of the segmentable

bus upstream of a particular connector and enable any expanders on portions of the segmentable bus downstream of the particular connector until the presence of another connector is determined.

7. (Original) The configurable storage array of claim 4, wherein the control logic is adapted to enable the all of the expanders on portions of the segmentable bus downstream of a particular connector in response to only one connector being identified.

8. (Original) The configurable storage array of claim 1, further comprising a plurality of expanders coupled between the segmentable bus and the input/output connectors.

9. (Original) The configurable storage array of claim 1, wherein the storage devices comprise tape drives.

10. (Original) The configurable storage array of claim 1, wherein the storage devices comprise hard disk drives.

11. (Original) The configurable storage array of claim 1, wherein the storage devices are hot-plug.

12. (Original) The configurable storage array of claim 1, wherein the control logic is adapted to determine the arrangement of connectors by monitoring the voltage state of a particular line in the input/output connectors.

13. (Original) The configurable storage array of claim 1, further comprising a plurality of switches associated with the input/output connectors, wherein a first subset of the switches is enabled in response to a connector being attached to the associated input/output connectors, a second subset of the switches is disabled in response to a connector not being attached to the associated

input/output connectors, and the control logic is adapted to determine the arrangement of connectors by monitoring the states of the first and second subsets of the switches.

14. (Original) The configurable storage array of claim I, wherein the segmentable bus comprises a small computer system interface (SCSI) bus.

15. (Previously presented) A method for configuring a storage array having a plurality of storage devices, comprising:

determining an arrangement of connectors coupled to input/output connectors of the storage array; and

grouping subsets of the storage devices onto isolated bus segments in the storage array based on the arrangement of connectors.

16. (Original) The method of claim 15, wherein the storage array includes a bus coupled to the storage devices, and grouping the subsets comprises segmenting the bus to define the isolated bus segments.

17. (Original) The method of claim 15, wherein determining the arrangement of connectors and grouping the subsets of the storage devices comprises determining the arrangement of connectors and grouping-the-subsets of the storage devices upon power up of the storage array.

18. (Original) The method of claim 15, wherein determining the arrangement of connectors and grouping the subsets of the storage devices comprises determining the arrangement of connectors and grouping the subsets of the storage devices in response to the activation of a reconfiguration switch on the storage array.

19. (Original) The method of claim 16, wherein segmenting the bus includes selectively enabling and disabling ones of a plurality of expanders separating portions of the bus.

20. (Original) The method of claim 19, wherein selectively enabling and disabling ones of the plurality of expanders comprises disabling one of the expanders on a portion of the bus upstream of a particular connector and enabling any expanders on portions of the bus downstream of the particular connector until the presence of another connector is determined.

21. (Original) The method of claim 19, selectively enabling and disabling ones of the plurality of expanders comprises enabling the all of the expanders on portions of the segmentable bus downstream of a particular connector in response to only one connector being identified.

22. (Original) The method of claim 16, further comprising enabling a plurality of expanders coupled between the bus and the input/output connectors.

23. (Original) The method of claim 15, wherein determining the arrangement of connectors comprises monitoring the voltage state of a particular line in the input/output connectors.

24. (Original) The method of claim 15, wherein the storage array further includes a plurality of switches associated with the input/output connectors, a first subset of the switches being enabled in response to a connector being attached to the associated input/output connectors, a second subset of the switches is disabled in response to a connector not being attached to the associated input/output connectors, and wherein determining the arrangement of connectors comprises monitoring the states of the first and second subsets of the switches.

25. (Previously presented) An apparatus, comprising:

a storage array having a plurality of storage devices;

means for determining an arrangement of connectors coupled to input/output connectors of the storage array; and

means for grouping subsets of the storage devices onto isolated bus segments in the storage array based on the arrangement of connectors.